ABSTRACT OF THE DISCLOSURE

To reduce the on-resistance in a semiconductor device, such as a trench lateral power MOSFET, a trench etching region forms a mesh pattern in which a first trench section, formed in an active region, and a second trench section, formed in a gate region for leading out gate polysilicon to a substrate surface, intersect each other. An island-like non-trench region, which is left without being subjected to etching, is divided into a plurality of smaller regions by one or more third trench section that connect with the first and second trench sections that form the mesh pattern. In each non-trench region, a contact section for connecting a drain region (or a source region) and an electrode is formed so as to be spread over all of the smaller regions in the non-trench region.